Consistent Processing and Long Term Stability of CdTe Devices

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ABSTRACT

A technology for processing of thin film CdS/CdTe devices has been developed in our laboratory. This in-line, continuous, pilot system enables unique processing steps and conditions not available with batch processing and allows the fabrication of a large number of devices. Results from the pilot scale system are applicable to systems processing larger areas.

Utilizing the pilot system, significant progress has been made towards demonstrating consistent stability (resistance to degradation) for thin film CdTe photovoltaics. We have repeatedly shown that devices with good stability can be produced if processed at the optimum set of conditions. Small changes in processes can lead to significant differences in device stability. Among the processing steps for fabrication of CdTe devices, the $CdCl_2$ treatment has a significant effect on performance and stability. A metric has been developed to predict the stability of devices at the time of device fabrication. Accelerated stress testing is ongoing. Extremely long duration stress testing (65°C, open circuit conditions for ~30,000 hours with 5 hours of illumination out of 8 hour cycle) has demonstrated that the rate of efficiency loss levels out with final efficiencies in the range of 8.5% ~ 9.5%.

A production prototype system for processing nominally 2MW/yr. is currently under construction. This system utilizes the process definition developed in the pilot system.

EXPERIMENTAL

Pilot scale fabrication system

The pilot scale system is a continuous, all in-line system where all device fabrication steps are performed in one vacuum boundary. These processing steps include glass heating, CdS and CdTe deposition, $CdCl_2$ heat treatment, back contact formation and back contact heat-treatment [1,2]. The system operates at 40m Torr N_2. The required base pressure for the system is only 10^{-3} Torr, allowing the use of low cost hardware. A residual gas analyzer (RGA) is used to monitor chamber gas composition. Process stations are nearly identical in design and construction. A schematic of the pilot scale is shown in Figure 1.

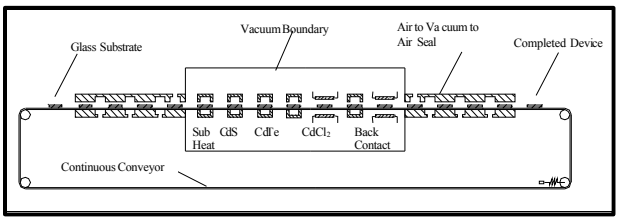

Fig. 1: Schematic of the 3.6 in. X 3.1 in. continuous in-line vacuum process.

An automated conveyor belt extends from air, through all the processing stations in vacuum and then back to air. The cycle time of each process station is 2 minutes, thus one substrate emerges from the system every 2 minutes. The substrate size is 3.6 x 3.1 inches. The pilot system has been used to process nearly 10,000 films and devices.

Initial device perforce and device structure

Devices have consistently been fabricated with 10.5 to 12.5% conversion efficiency with an NREL verified 12.44% and 71% fill factor. The highest efficiency measured on the devices produced with the pilot system is 13.0% on unmodified Pilkington TEC 15 glass.

The device structure is glass/SnO_x:F/ CdS/CdTe/carbon/nickel. Nominal CdS thickenss is 0.2 microns and CdTe layer thickness is between 1.5 and 1.9 microns. The substrates are soda lime glass with a tin oxide coating from Pilkington (TEC 15); the tin oxide is unmodified. These devices had no anti-reflection, buffer or intrinsic layers. The back contact is formed in vacuum through the vapor deposition of a copper compound followed by annealing [1,2]. Metallization is performed by low cost spray processing outside of vacuum. The sprayed films consist of conductive particulates in acrylic binders. Two layers are used, one containing carbon applied to the CdTe surface and the other containing nickel applied on the carbon layer. During processing the ambient gas was dry N_2 with a partial pressure of oxygen in the range of 0.5-2%.

All processing steps up to metallization are performed in-line and continuously in a single vacuum chamber. There was no wet processing and no chemical etch step. The carbon metallization contains no intentional copper.

For the devices in this work which were studied for stability performance the $CdCl_2$ treatment was varied. Devices from the same process fabrication run, with the same $CdCl_2$ treatment, were fabricated both with and without the application of the Cu containing back contact. In the cases where the contact processing was performed it was nominally the same in all cases. The JV parameters were measured on both types of devices and fully processed cells with the Cu containing back contact were placed in indoor accelerated stress environments to measure stability performance.

$CdCl_2$ treatment

For the devices in this study, the $CdCl_2$ treatment was performed immediately following the CdTe deposition in the pilot system. The treatment consists of an exposure of the CdS/CdTe films to a $CdCl_2$ vapor flux for 2 minutes. A $CdCl_2$ film was deposited on the surface of the CdTe layer. The substrate temperature was approximately 512° C on entry to the $CdCl_2$ vapor source. The substrate temperature dropped to close to 400° C at the end of the $CdCl_2$ vapor flux treatment step. The substrate temperature was controlled with a heater located over the substrate. After exposure to $CdCl_2$ flux the substrate and films were annealed at ~ 400° C for 2 minutes. Any $CdCl_2$ film that was deposited was re-sublimed away from the CdTe surface during this anneal step.

The $CdCl_2$ treatment flux, substrate temperature and annealing temperature were varied. The variation of the $CdCl_2$ treatment was part of a process optimization study extending over 2 years and included more than 500 cells.

RESULTS

Correlation of the $CdCl_2$ treatment and device stability

The stability of CdTe devices is of significant interest [3,4]. The development of a metric or methodology to ensure consistent stability has been the focus of significant effort. A relationship between initial, unstressed device performance and long-term stability has been established. The stability of devices with intentional copper under accelerated stress can be qualitatively predicted using light JV data from devices processed identically but without the intentional addition of copper. This relationship fits all relevant data for devices processed with the pilot system.

Figure 2 shows the plot of short circuit current vs. open circuit voltage for devices processed without intentional copper and measured before application of stress. The devices have varied $CdCl_2$ treatment. There is an obvious correlation between the JV data in Figure 2 and the stability of devices in Figure 3. This shows that the fabrication processing, particularly the $CdCl_2$ treatment, has a large effect on the device stability. The devices denoted by the open diamonds (6430 and 31) show the highest combined Jsc and Voc. Figure 3 shows the stability of devices processed nearly identically to those in Figure 2 except for the intentional addition of copper to form the back contact. (Similar process conditions are denoted by the same point shape in both Figures 2 and 3) As seen in Figure 3, the most stable devices are those with the open diamonds (6652 and 6549) which, except for the intentional addition of copper, are nearly identical to 6430 in Figure 2. Similarly, the Jsc and Voc for other devices in Figure 2 are predictive of the stability performance shown in Figure 3.

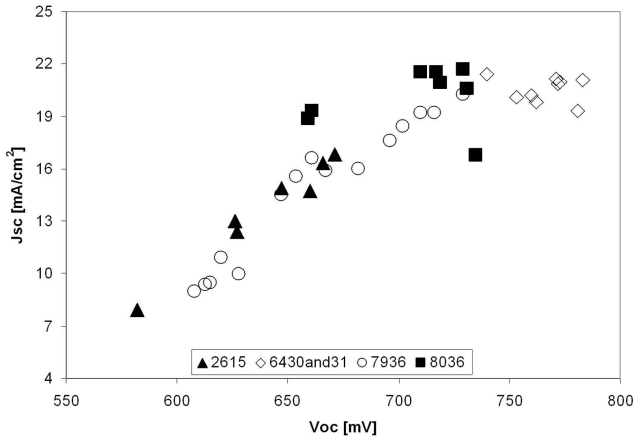

Fig 2: Current density vs. open circuit voltage scatter plot for devices with varied $CdCl_2$ treatment but with no Cu back contact. The insert shows the substrate numbers.

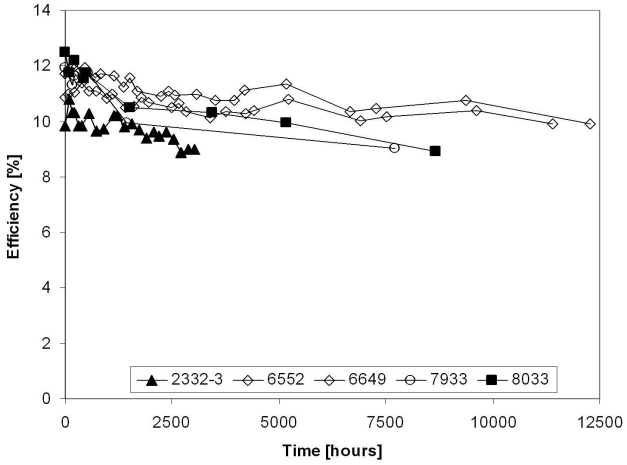

Fig. 3: Indoor accelerated stability plot for devices with Cu back contact. Markers for devices with similar $CdCl_2$ treatment are the same in Figure 2 and Figure 3.

In contrast, the initial performance of devices made with intentional copper is not as predictive. Figure 4 shows the Voc vs. Jsc of devices processed at similar conditions with the devices of Figure 2 except with intentional copper. Similar process conditions (other than copper) are denoted by the same point shape in Figures 2, 3 and 4. Comparing Figure 2 and Figure 4

demonstrates that the Voc and Jsc of the devices without intentional copper are more effective at predicting device stability.

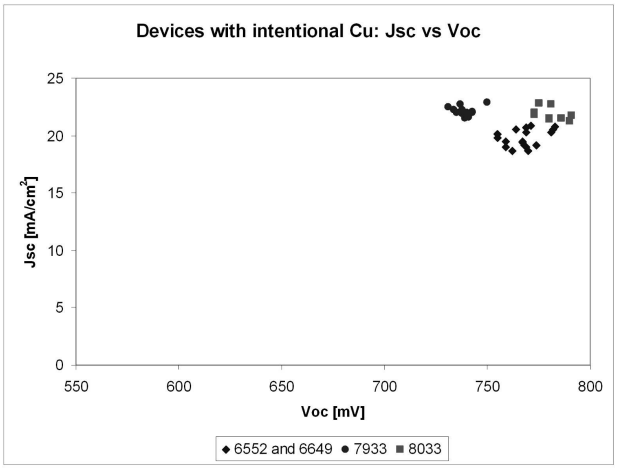

Figure 4: Short circuit current (Jsc) vs. open circuit voltage (Voc) of devices WITH intentional copper measured at simulated AM 1.5 illumination. All measurements taken are before stress.

Very long term accelerated stress testing

Some of our devices have undergone accelerated stress testing for almost 3.5 years. The stress conditions are 65° C, ~ 1000 W/m^2 illumination (cycled 5 hr. on/ 3 hr. off), open circuit bias, with a desiccated ambient.

Cells are removed periodically from the lightsoak environment and the JV parameters are measured using calibrated ELH lamp illumination. Cells were in groups of 6-9 taken from the same process run and conversion efficiencies are averaged across the group. Cells processed at optimum conditions have the best stability.

The efficiency loss follows an exponential decay described by the function:

$$\eta = \alpha \cdot \exp\left(\frac{-t}{\lambda}\right) + \eta_{sat} \quad [1]$$

Where t is the total time and alpha, lamda, and the saturation efficiency (η_{sat}) are constants determined by the fit. For the first ~10,000 hours of light soaking the efficiency loss over time is relatively rapid. At approximately 20~25,000 total hours, the efficiency loss levels. The data of average efficiency vs. stress time is shown in Figure 5 along with the calculated exponential decay curves. The curve fits are statistical and no degradation mechanism is assumed. The data in Figure 5 was smoothed using a Savatzky-Golay 4th order polynomial routine. The line fit with equation [1] was made using the software Psi Plot 7.5. The curve fit correlation parameters (a measure of how accurately the curve approximates the data) ranged from R = 0.86 ~ 0.99 for the fits shown. Maintaining devices at open circuit during stress testing (the condition of the devices in Figure 5) is generally considered to be the most severe condition [5]; it is expected that devices operating in the field (at max. power conditions) will have better stability performance.

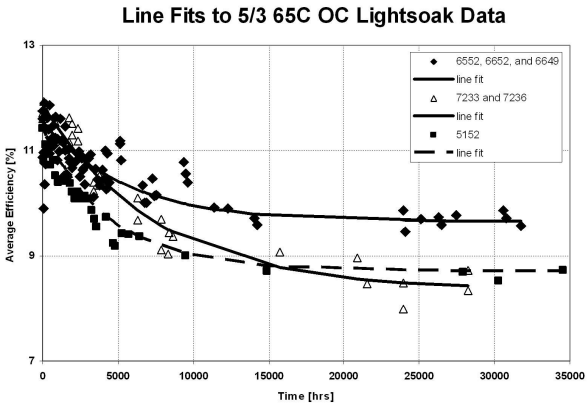

Fig. 5**:** Long term stability plot. Each line represents an average of at least six devices.

Consistent processing

The development of hardware and the determination of optimum conditions for the CdS, CdTe and $CdCl_2$ processing steps, consistently over long duration system operation has been a focus of effort. This has led to the development of an optimum, baseline process for all PV fabrication steps up to the back contact formation. This baseline process has been repeated for over 9 hours of operation with the same source charge. The Voc and Jsc parameters of devices with no intentional copper (fabricated up to but not including the back contact processing) have remained consistent for over this 9 hour time. This is a significant result because the $CdCl_2$ process conditions are a dominant factor in determining device performance and stability. As shown above, the Voc and Jsc of devices with no intentional copper can be used to predict the stability of fully processed devices. Using this metric, this repeatable, baseline process setup will produce devices with good long term stability.

Process modules within the pilot and prototype production systems are designed for repeatability and long term operation. Within the pilot system, the CdS, CdTe and $CdCl_2$ vapor sources have continued to operate very consistently for over 9 hours without replenishment or alteration of the source charge. These process modules have proven to be quite repeatable and easy to control. The target thickness for the CdS/CdTe combined was 1.9 to 1.95 microns. The results of 8 process runs (each run is over an hour) yielded thickness between 0.125 micron below and 0.5 micron above the target. The CdTe vapor source temperature was intentionally varied only 1 °C during this time. This repeatability is extremely valuable for CdTe PV process development.

Development of the production prototype system

The pilot system described above has been used to determine the optimum process conditions that result in stable, efficient PV devices. The feasibility of processing commercial size modules was demonstrated. This was accomplished through the construction of the first portion of the production prototype system. The complete system is currently under construction. Large area solar cell processing modules (process heads) for the deposition and processing of the semiconductor films have been designed. A significant advantage of this technology is that the process modules are nearly identical for all vacuum process steps. Two stations have been constructed and installed and tested for mechanical, electrical and thermal performance with excellent results. The process stations designed for continuous running for 40 hours or more without reloading. Thermal uniformity of +/- 1.5 deg. C was measured for a temperature of 400 °C. The system has been tested for a continuous 78 hour thermal run (without source charge).

This system was constructed to demonstrate the ability to scale our technology. In addition, the system was designed to be part of the hardware for a production prototype used for processing 16x16 inch modules. These modules will nominally produce 10 W of power. (10 W modules are an existing commercial product.) 10 W modules can be connected together for higher power requirements. The system is designed to operate for long duration and is able to withstand the rigors of full manufacturing. However, the current system is only designed to process the devices through the CdS, CdTe semiconductor deposition and the $CdCl_2$ treatment. (Please see schematic in Figure 1.) This system is referred to as the "semiconductor subsystem" and was designed and constructed with support from DOE-EERE. Recently, DOE has provided support to complete the system. This project includes 50% cost share from our industrial partner, National Starch and Chemical (NSC).

Completing this system will result in a full PV manufacturing production prototype system. When operated in full production mode, the production prototype system is capable of producing 2 million watts (2 MW) of PV a year**.**

CONCLUSIONS

A continuous in-line technology has been developed to improve the processing of CdS/CdTe thin film PV. A pilot system has been used to demonstrate consistent device performance and stability and to develop process conditions for systems processing larger areas. A nominal 2 MW/yr. production prototype is currently being constructed.

The $CdCl_2$ treatment is of significant importance for determining the stability of CdTe devices. Minor variations in the $CdCl_2$ treatment lead to significant changes in device stability. Devices fabricated with optimum $CdCl_2$ treatment show better stability under accelerated indoor stress. The stability of devices with intentional copper under accelerated stress can be qualitatively predicted using light JV data from devices processed identically but without the intentional addition of copper. This relationship fits all relevant data for devices processed with the pilot system. In contrast, the initial performance of devices with intentional copper is not as predictive.

Extremely long duration stress testing at 65°C, open circuit conditions for ~30,000 hours with 5 hours of illumination out of 8 hour cycle, has demonstrated that the rate of efficiency loss levels out. Final efficiencies are in the range of 8.5% ~ 9.5%. Since open circuit bias is generally the most stressful condition, these should be considered lower limit values for what may be seen in outdoor conditions.

Consistent processing has been demonstrated over the course of 8 processing runs. Over 9 hours of process time the CdS/CdTe film thickness was maintained at 1.925 μ (+0.5 μ / - 0.125 μ). The Voc and Jsc of devices measured after the $CdCl_2$ treatment and with no Cu back contact are consistent over the same 9 hour process time frame.

ACKNOWLEDGEMENTS

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